



Sheet 1 of 14

U.S. Department of Commerce, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Pak Shing Chau
		Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"		Examiner Name: Bayard, Emmanuel
		Attorney Docket No.: RA-194

#### U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
ZM	A	4,481,625	11/06/84	Roberts, et al	370	85	
1	B	5,534,795	07/09/96	Wert, et al	326	81	RECEIVED
	C	5,534,798	07/09/96	Phillips, et al	326	108	NOV 14 2003
	D	5,663,663	09/02/97	Cao, et al	326	81	Technology Center 2600
	E	5,751,168	05/12/98	Speed, III et al	326	83	
	F	5,757,712	05/26/98	Nagel, et al	365	226	
	G	5,867,010	02/02/99	Hinedi, et al	323	282	
	H	5,973,508	10/26/99	Nowak, et al	326	81	
	I	5,986,472	11/16/99	Hinedi, et al	326	68	
	J	6,097,215	08/01/00	Bialas Jr., et al	326	68	
	K	6,140,841	10/31/00	Suh	326	60	
	L	6,160,421	12/12/00	Barna	326	63	
	M	4,748,637	05/31/88	Bishop, et al	375	7	
	N	5,254,883	10/19/93	Horowitz, et al	307	443	
	O	5,608,755	03/04/97	Rakib	375	219	
	P	5,546,042	08/13/96	Tedrow, et al	327	538	
	Q	5,194,765	03/16/93	Dunlop, et al	307	443	
AM	R	5,254,883	10/19/93	Horowitz, et al	307	443	
Examiner			Date Considered <u>5/6/05</u>				

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



Sheet 2 of 14

U.S. Department of Commerce, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Pak Shing Chau
		Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"		Examiner Name: Bayard, Emmanuel
		Attorney Docket No.: RA-194

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
AB	S	5,513,327	04/30/96	Farmwald, et al	395	309	
	T	5,023,488	06/11/91	Gunning	307	475	
	U	5,483,110	01/09/96	Koide, et al	307	147	RECEIVED
	V	5,287,108	02/15/94	Mayes, et al	341	156	NOV 14 2003
	W	5,977,798	11/02/99	Zerbe	329	98	Technology Center 2600
	X	RE30,182	12/25/79	Howson	325	42	
	Y	2,912,684	11/10/59	F.G. Steele	340	347	
	Z	3,051,901	08/28/62	R.E. Yaegar	325	38	
	AA	3,078,378	02/19/63	C.H. Burley, et al	307	88.5	
	AB	3,267,459	08/16/66	J.S. Chomicki, et al	340	347	
	AC	3,484,559	12/16/69	D.F. Rigby	179	18	
	AD	3,508,076	04/21/70	R.O. Winder	307	235	
	AE	3,510,585	05/05/70	R.B. Stone	325	38	
	AF	3,560,856	02/02/71	Hisashi, Kaneko	375	292	
	AG	3,569,955	03/09/71	Maniere	340	347	
	AH	3,571,725	03/23/71	Kaneko, et al	328	14	
	AI	3,587,088	06/22/71	Frana szek	340	347	
AB	AJ	3,648,064	03/07/72	Mukai, et al	307	213	

Examiner

Date Considered

5/6/05

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



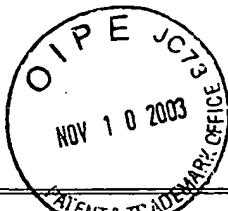
Sheet 3 of 14

U.S. Department of Commerce, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Pak Shing Chau
		Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"		Examiner Name: Bayard, Emmanuel
		Attorney Docket No.: RA-194

U. S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
X/S	AK	3,697,874	10/10/72	Kaneko	325	38 A	
11	AL	3,731,199	05/01/73	Tazaki, et al	325	38 A	
	AM	3,733,550	05/15/73	Tazaki, et al	325	38 A	
	AN	3,753,113	08/14/73	Maruta, et al	325	38 A	NOV 14 2003
	AO	3,754,237	08/21/73	de Laage de Meux	340	347 DD	Technology Center 2600
	AP	3,761,818	09/25/73	Tazaki, et al	325	38 A	
	AQ	3,772,680	11/13/73	Kawai, et al	340	347 DD	
	AR	3,798,544	03/19/74	Norman	325	38 A	
	AS	3,832,490	08/27/74	Leonard	178	68	
	AT	3,860,871	01/14/75	Hinoshita, et al	325	38 B	
	AU	3,876,944	04/08/75	Mack, et al	325	141	
	AV	3,927,401	12/16/75	McIntosh	340	347 DD	
	AW	3,978,284	08/31/76	Yoshino, et al	178	69.5 R	
	AX	3,988,676	10/26/76	Whang	325	38 A	
	AY	4,038,564	07/26/77	Hakata	307	205	
	AZ	4,070,650	01/24/78	Ohashi, et al	340	172	
	BA	4,086,587	04/25/78	Lender	340	347 DD	
X/S	BB	4,097,859	06/27/78	Looschen	340	347 DD	
Examiner			Date Considered	5/6/05			

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



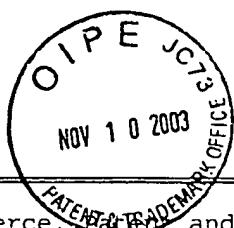
Sheet 4 of 14

U.S. Department of Commerce, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Pak Shing Chau
		Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"		Examiner Name: Bayard, Emmanuel
		Attorney Docket No.: RA-194

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
✓	BC	4,131,761	12/26/78	Giusto	179	15 BY	
✓	BD	4,181,865	01/01/80	Kohyama	307	361	
	BE	4,373,152	02/08/83	Jacobsthal	340	347	NOV 14 2003
	BF	4,382,249	05/03/83	Jacobsthal	340	347 DD	Technology Center 2600
	BG	4,403,330	09/06/83	Meyer	375	4	
	BH	4,408,135	10/04/83	Yuyama, et al	307	474	
	BI	4,408,189	10/04/83	Betts, et al	340	347 DD	
	BJ	4,528,550	07/09/85	Graves, et al	340	347 DD	
	BK	4,438,491	03/20/84	Constant	364	200	
	BL	4,571,735	02/18/86	Furse	375	20	
	BM	4,602,374	07/22/86	Nakamura, et al	375	17	
	BN	4,628,297	12/09/86	Mita, et al	340	347 DD	
	BO	4,779,073	10/18/88	Iketani	341	55	
	BP	4,805,190	02/14/89	Jaffre, et al	375	17	
	BQ	4,821,286	04/11/89	Graczyk, et al	375	4	
	BR	4,823,028	04/18/89	Lloyd	307	355	
✓	BS	4,841,301	06/20/89	Ichihara	341	126	
✓	BT	4,860,309	08/22/89	Costello	375	17	
Examiner			Date Considered				

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



Sheet 5 of 14

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
<i>AS</i>	BU	4,875,049	10/17/89	Yoshida	341	159	
<i>1</i>	BV	4,888,764	12/19/89	Haug	370	85.1	RECEIVED
	BW	5,003,555	03/26/91	Bergmans	375	12	NOV 14 2003
	BX	5,045,728	09/03/91	Crafts	307	475	Technology Center 2600
	BY	5,115,450	05/19/92	Arcuri	375	7	
	BZ	5,121,411	06/09/92	Fluharty	375	20	
	CA	5,172,338	12/15/92	Mehrotra, et al	365	185	
	CB	5,191,330	03/02/93	Fisher, et al	341	56	
	CC	5,230,008	07/20/93	Duch, et al	375	19	
	CD	5,243,625	09/07/93	Verbakel, et al	375	17	
	CE	5,280,500	01/18/94	Mazzola, et al	375	17	
	CF	5,295,155	03/15/94	Gersbach, et al	375	4	
	CG	5,315,175	05/24/94	Langner	307	443	
	CH	5,331,320	07/19/94	Cideciyan, et al	341	56	
	CI	5,408,498	04/18/95	Yoshida	375	286	
<i>U</i>	CJ	5,425,056	06/13/95	Maroun, et al	375	316	
	CK	5,426,739	06/20/95	Lin, et al	395	325	
<i>AS</i>	CL	5,438,593	08/01/95	Karam, et al	375	317	
Examiner		Date Considered					

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



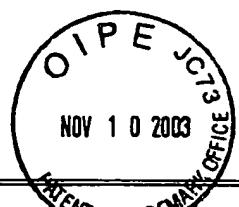
Sheet 6 of 14

U.S. Department of Commerce, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Pak Shing Chau
		Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"		Examiner Name: Bayard, Emmanuel
		Attorney Docket No.: RA-194

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
<i>a-1</i>	CM	5,459,749	10/17/95	Park	375	286	
<i>1</i>	CN	5,471,156	11/28/95	Kim, et al	326	60	RECEIVED
	CO	5,473,635	12/05/95	Chevroulet	375	287	NOV 14 2003
	CP	5,525,983	06/11/96	Patel, et al	341	57	Technology Center 2600
	CQ	5,663,631	09/02/97	Kajiura, et al	322	29	
	CR	5,640,605	06/17/97	Johnson, et al	395	881	
	CS	5,684,833	11/04/97	Watanabe	375	286	
	CT	5,740,201	04/14/98	Hui	375	286	
	CU	5,793,815	08/11/98	Goodnow, et al	375	286	
	CV	5,793,816	08/11/98	Hui	375	286	
	CW	5,796,781	08/18/98	DeAndrea, et al	375	288	
	CX	5,825,825	10/20/98	Altmann, et al	375	293	
	CY	5,872,468	02/16/99	Dyke	327	72	
	CZ	5,892,466	04/06/99	Walker	341	57	
	DA	5,898,734	04/27/99	Nakamura, et al	375	287	
	DB	5,917,340	06/29/99	Manohar, et al	326	82	
	DC	5,933,458	08/03/99	Leurent, et al	375	317	
<i>a-h</i>	DD	5,942,994	08/24/99	Lewiner, et al	341	56	
Examiner <i>S-4</i>			Date Considered <i>5/6/03</i>				

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



Sheet 7 of 14

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

#### U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
<i>x-16</i>	DE	5,946,355	08/31/99	Baker	375	286	—
<i>1</i>	DF	5,949,280	09/07/99	Sasaki	329	303	<b>RECEIVED</b>
	DG	5,969,579	10/19/99	Hartke, et al	332	116	NOV 14 2003
	DH	5,969,648	10/19/99	Garnett	341	56	—
	DI	6,018,550	01/25/00	Emma, et al	375	317	Technology Center 2600
	DJ	6,038,260	03/14/00	Emma, et al	375	259	—
	DK	6,049,229	04/11/00	Manohar, et al	326	83	—
	DL	6,052,390	04/18/00	Deliot, et al	370	258	—
	DM	6,067,326	05/23/00	Jonsson, et al	375	286	—
	DN	6,078,627	06/20/00	Crayford	375	286	—
	DO	6,048,931	04/11/00	Fujita, et al	525	67	—
	DP	6,094,461	07/25/00	Heron	375	317	—
	DQ	6,101,561	08/08/00	Beers, et al	710	66	—
	DR	6,114,979	09/05/00	Kim	341	57	—
	DS	6,122,010	09/19/00	Emelko	348	461	—
	DT	6,140,841	10/31/00	Suh	326	60	—
<i>16</i>	DU	6,195,397	02/27/01	Kwon	375	288	—
<i>x-16</i>	DV	5,023,841	06/11/91	Akroot, et al	365	205	—
Examiner <i>[Signature]</i>		Date Considered					<i>11/18/05</i>

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



Sheet 8 of 14

U.S. Department of Commerce, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Pak Shing Chau
		Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"		Examiner Name: Bayard, Emmanuel
		Attorney Docket No.: RA-194

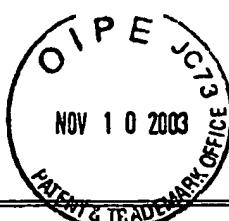
#### U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
<i>AS</i>	DW	5,126,974	06/30/92	Sasaki, et al	365	207	
<i>AS</i>	DX	5,153,459	10/06/92	Park, et al	307	452	<b>RECEIVED</b>
	DY	5,373,473	12/13/94	Okumura	365	208	NOV 14 2003
	DZ	5,508,570	04/16/96	Laber, et al	327	563	
	EA	5,734,294	03/31/98	Bezzam, et al	327	552	Technology Center 2600
	EB	6,307,824	10/23/01	Kuroda, et al	369	53.11	
	EC	4,280,221	07/21/81	Chun, et al	375	17	
	ED	4,620,188	10/28/86	Sengchanh	340	825.87	
	EF	4,825,450	04/25/89	Herzog	375	17	
	EG	5,259,002	11/02/93	Carlstedt	375	38	
	EH	5,412,689	05/02/95	Chan, et al	375	288	
	EI	5,553,097	09/03/96	Dagher	375	240	
	EJ	5,644,253	07/01/97	Takatsu	326	35	
	EK	5,761,246	06/02/98	Cao, et al	375	287	
	EL	5,864,584	01/26/99	Cao, et al	375	244	
	EM	6,005,895	12/21/99	Perino, et al	375	288	
	EN	6,094,075	07/25/00	Garrett, Jr. et al	327	108	
<i>AS</i>	EO	5,046,050	09/03/91	Kertis	365	208	

Examiner

Date Considered *9/17/05*

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



Sheet 9 of 14

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Group Art Unit: 2631 Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

### Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
✓	EP	EP 0 463 316 A1	02.01.92	EP	H04L 12	40	X	
	EQ	EP 0 482 392 A2	10.02.91	EP	H04L 25	08	X	
	ER	JP 04044691 A	02.14.92	JP	G11C 007	00		X
	ES	DE 43 20 930 A1	01.05.95	DE	H04L0 25	49		X
	ET	EP 0 094 624 A2	11.23.83	EP	H04L0 25	49		X
	EU	EP 0 490 504 A2	17.06.92	EP	H04L 25	49	X	
	EV	JP 54051343 A	04.23.79	JP	G06F 005	00		X
	EW	JP 56164650 A	12.17.81	JP	H04L 011	00		X
	EX	JP 59036465 A	02.28.84	JP	H04L 027	02		X
	EY	JP 60087551 A	05.17.85	JP	H04L 025	49		X
	EZ	JP 60194647 A	10.03.85	JP	H04L 013	00		X
	FA	JP 02128201 A	05.16.90	JP	G05B 019	05		X
✓	FB	JP 02140676 A	05.30.90	JP	G01R 031	28		X
✓	FC	58-54412(A) (cover sheet only)	03.31.83	JP	G05 F1	56	X	

Examiner

Date Considered

4/17/05

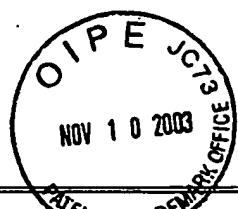
\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

RECEIVED

NOV 14 2003

Technology Center 2600

Sheet 10 of 14



U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

## Foreign Patent Documents

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
✓	FD	JP 05143211 A	06/11/93	JP	G06F 003	00		X
✓	FE	JP 08202677 A	08/09/96	JP	G06F 015	78		X
✓	FF	JP 08286943 A	11/01/96	JP	G06F 011	22		X
✓	FG	JP 09181778 A	07/11/97	JP	H04L 027	06		X
✓	FH	WO 96/31038 A1	10/03/96	EP	H04L 025	49		X
✓	FI	WO 98/33306	07/30/98	JP	H03K 019	20		X
✓	FJ	JP 62051329 A	03/06/87	JP	H04L 007	02		X
✓	FK	JP 58070662 A	04/27/83	JP	H04L 025	49		X
✓	FL	JP 54060850 A	05/16/79	JP	H03K 004	02		X
✓	FM	EP 0 352 869 A2	01/31/90	EP	G01V 1	22	X	
✓	FN	WO 95/31867	11/23/95	PCT CA	H04M 1	24		X
✓	FO	JP 10200345 A	07/31/98	JP	H03F 003	45		X
✓	FP	WO 99/10982	03/04/99	PCT CA	H03K 19	0175		X

Examiner

Date Considered

4/17/05

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

RECEIVED

NOV 14 2003

Technology Center 2600

Sheet 11 of 14



U.S. Department of Commerce, <del>PATENT &amp; TRADEMARK OFFICE</del>	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

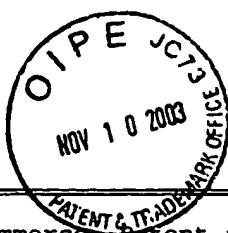
<i>✓/S</i>	FR	IBM, Disclosure entitled, "Servo Control of Analog Power Supplies Purpose Interface Card", 4/1/1993, Vol. 36, Issue 4, pages 283-286
<i>✓</i>	FS	Sidiropoulos, Stefanos, et al. "A 700 Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers", IEEE Journal of Solid-State Circuits; Vol. 32, No.5, May 1997; pp. 681-690
	FT	Donnelly, Kevin S. et al. "A 660 MB/s Interface Megacell Portable Circuit in 0.3 um-0.7 um CMOS ASIC", IEEE Journal of Solid State Circuits; Vol. 31, No.12; December 1996, pp. 1995-2003
	FU	Allen, Arnold O., "Probability, Statistics, and Queueing Theory with Computer Science Applications", 2 <sup>nd</sup> Edition, CH 7; pp. 450, 458-459
	FV	Chappell, Terry I. et al. "A 2ns Cycle, 4ns Access 512kb CMOS ECL SRAM", IEEE International Solid State Circuits Conference 1991; pp. 50-51
	FW	Pilo, Harold et al., "A 300 MHz 3.3V 1 Mb SRAM Fabricated in a 0.5 um CMOS Process", IEEE International Solid State Circuits Conference 1996; pp. 148-149
	FX	Schumacher, Hans-Jurgen et al., "CMOS Subnanosecond True-ECL Output Buffer", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1; February 1990 pp. 150-154.
	FY	Yang, Tsen-Shau et al., "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM", IEEE Journal of D-State Circuits; Vol. 23, No. 5; October 1988; pp. 1030-1040
	FZ	Sidiropoulos, Stefanos, et al. "A 700 Mbps/pin CMOS Signalling Interface Using Current Integrating Receivers", IEEE Symposium on VLSI Circuits Digest of Technical Papers, 1996; pp 142-143
	GA	Bazes, Mel, "Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers", IEEE Journal of Solid State Circuits, Vol. 26 No. 2., February 1991
	GB	Ishibe, Manabu et al., "High-Speed CMOS I/O Buffer Circuits", IEEE Journal of Solid State Circuits, Vol. 27, No. 4, April 1992
	GC	Lee, James M. et al., "A 80ns 5V-Only Dynamic RAM", ISSCC Proceedings, Paper 12.2 ISSCC 1979.
<i>✓</i>	GD	Seki, Teruo et al., "A 6-ns 1-Mb CMOS SRAM with Latched Sense Amplifier", IEEE Journal of Solid State Circuits, Vol. 28, No. 4., April 1993
<i>✓/S</i>	GE	Kobayashi, Tsuguo et al., "A Current-Controlled Latch Sense Amplifier and a Static Power-Saving Input Buffer for Low-Power Architecture", IEEE Journal of Solid State Circuits, Vol. 28, No. 4., April 1993

Examiner

Date Considered

*4/17/05*

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



RECEIVED

NOV 14 2003

Technology Center 2600

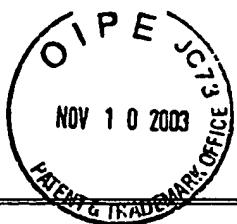
Sheet 12 of 14

U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

X/S	GF	Tomasini, Luciano et al. "A Fully Differential CMOS Line Driver for ISDN", IEEE Journal of Solid State Circuits, Vol. 25, No. 2., April 1990. Pages 546-585.
1	GG	Farjad-Rad, Ramin et al., "A 0.4 um CMOS 10-Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter", IEEE Journal of Solid State Circuits, Vol. 34 No. 5, pp. 580-585, May 1999.
	GH	Yeung, Evelina et al., "A 2.4Gbps Per Pin Simultaneous Bidirectional Parallel Link with Per Pin Skew Compensation," ISSCC 2000, in press as of 1-9-2000.
	GI	Portmann C. et al., "A Multiple Vendor 2.5-V DLL for 1.6-GB/s RDRaMs", IEEE VLSI Circuits Symposium, June 1999.
	GJ	Moncayo Alfredo, "Bus Design and Analysis at 500 MHz and Beyond", Presented at the High-Performance System Design Conference, 1995.
	GK	Lau, Benedict et al., " A 2.6-Gbyte/s Multipurpose Chip-to-Chip Interface", IEEE Journal of Solid-State Circuits, Vol. 33, No. 11 pp. 1617-1626, November 1998.
	GL	Current, Wayne K., "Current-Mode CMOS Multiple-Valued Logic Circuits", IEEE Journal of Solid-State Circuits, Vol. 29, No. 2, pp. 95-107, February 1994.
	GM	Dally, William J. et al., "Digital Systems Engineering", Cambridge University Press, New York, NY, 1998, Index, pp. 344-347 and pg. 352.
	GN	Farjad-Rad, Ramin et al., "An Equalization Scheme for 10Gb/s 4-PAM Signaling Over Long Cables," Presentation Center for Integrated Systems, Department of Electrical Engineering, Stanford University, July 28, 1997
	GO	Vranesic, Z.G. "Multivalued Signalling in Daisy Chain Bus Control", Proceedings of the Ninth International Symposium on Multiple-Valued Logic, Bath, England, pp. 14-18
	GP	IBM Technical Disclosure Bulletin, "Use of Multibit Encoding to Increase Linear Recording Densities in Serially Recorded Records," June 1967. pp. 14-15
1	GQ	IBM Technical Disclosure Bulletin, "Coding for Data Transmission", January 1968, pp. 1295-1296
	GR	IBM Technical Disclosure Bulletin, "Clock Recovery Circuit," July 1969, pp. 219-220
X/S	GS	IBM Technical Disclosure Bulletin, "Transmission by Data Encoding," November 1970, pg. 1519
Examiner		Date Considered  4/17/05

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



RECEIVED

NOV 14 2003

Technology Center 2600

Sheet 13 of 14

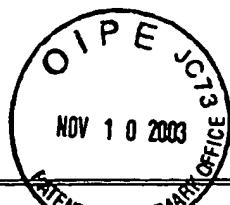
U.S. Department of Commerce, Patent and Trademark Office	Serial No.: 09/654,643
	Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	First Named Inventor: Pak Shing Chau
	Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"	Examiner Name: Bayard, Emmanuel
	Attorney Docket No.: RA-194

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

a/s	GT	IBM Technical Disclosure Bulletin, "Bidirectional Communications within a Binary Switching System", February 1976, pp. 2865-2866
1	GU	IBM Technical Disclosure Bulletin, "Multilevel Bidirectional Signal Transmission", February 1976, pp. 2867-2868.
	GV	IBM Technical Disclosure Bulletin, "Multilevel Signal Transfers," October 1978, pp. 1798-1800
	GW	IBM Technical Disclosure Bulletin, "Circuit for Multilevel Logic Implementation", February 1981, pp 4206-4207
	GX	IBM Technical Disclosure Bulletin, "Multi Level Logic Testing", April 1983, pp. 5903-5904
	GY	IBM Technical Disclosure Bulletin, "Push-Pull Multi-Level Driver Circuit for Input-Output Bus", September 1985, pp. 1649-1650
	GZ	IBM Technical Disclosure Bulletin, "Multilevel CMOS Sense Amplifier", August 1986, pp. 1280-1281
	HA	IBM Technical Disclosure Bulletin, "Multi-Level Encoded High Bandwidth Bus", November 1992, pp. 444-446
	HB	IBM Technical Disclosure Bulletin, "High Speed Complimentary Metal Oxide Semiconductor Input/Output Circuits", February 1995, pp. 111 of 111- 114.
	HC	IBM Technical Disclosure Bulletin, "Common Front End Bus for High-Performance Chip-to-Chip Communication", April 1995, pp. 443-444
	HD	IBM Technical Disclosure Bulletin, "High Performance Impedance Controlled CMOS Drive", April 1995, pp. 445-446
	HE	IBM Technical Disclosure Bulletin, "3-State Decoder for External 3-State Buffer", April 1995, pg. 477
a/s	HF	Matick, Richard E., "Transmission Lines for Digital and Communication Networks: An Introduction to Transmission Lines, High-Frequency and High-Speed Pulse Characteristics and Applications," IEEE Press, New York, 1995, pp. 268-269

Examiner	Date Considered
----------	-----------------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



RECEIVED

NOV 14 2003

Technology Center 2600

Sheet 14 of 14

U.S. Department of Commerce, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/00
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		First Named Inventor: Pak Shing Chau
		Group Art Unit: 2631
"Low-Latency Equalization in Multi-Level, Multi-Line Communication Systems"		Examiner Name: Bayard, Emmanuel
		Attorney Docket No.: RA-194

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>J-H</i>	HG	Singh, Adit D. "Four Valued Buses for Clocked CMOS VLSI Systems", Proceedings of the Seventeenth International Symposium on Multiple-Valued Logic, The Computer Society of the IEEE. Boston, Massachusetts, May 26-28, 1987, pp. 128-133
<i>D/H</i>	HI	Smith, K.C. "The Prospects for Multivalued Logic: A Technology and Applications View", IEEE Transactions on Computers 1981, Vol. C-30, No. 9, pp. 619-634
<i>R/B</i>	HJ	Thirion, Walter, "10 Gig PMD Technologies", IEEE Plenary, Kauai, Hawaii, November 1999. 10 pages.
	HK	
	HL	
	HM	
	HN	
	HO	
	HP	
	HQ	
	HR	
	HS	
	HT	

Examiner

Date Considered

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



Sheet 1 of 1

U. S. DEPARTMENT OF COMMERCE, Patent and Trademark Office		Serial No.: 09/654,643
		Filing Date: 09/05/2000
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Inventors: Pak Shing Chau, et al.
		Group Art Unit: Unknown
"LOW-LATENCY EQUALIZATION IN MULTI-LEVEL, MULTI-LINE COMMUNICATION SYSTEMS"		Examiner Name: Unknown
		Attorney Docket No.: RA-194

#### U. S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date, If Appropriate
	A						RECEIVED
	B						SEP 03 2003
	C						
	D						Technology Center 2600
	E						

#### Foreign Patent Documents

							Translation	
		Document Number	Date	Country	Class	Subclass	Yes	No
	F							

#### OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>xis</i>	G	Raghavan, S.A. et al. "Nonuniformly Spaced Tapped-Delay-Line Equalizers," IEEE Transactions on Communications, Vol. 41, No. 9, September 1993, pp 1290-1295.
<i>KIS</i>	H	Ariyavitsakul, Sirikit et al. "Reduced-Complexity Equalization Techniques for Broadband Wireless Channels," IEEE Journal on Selected Areas in Communications, Vol. 15, No. 1, January 1997, pp 5-15.
<i>xis</i>	I	Sidiropoulos, Stefanos et al. "A 700-Mb/s/pin CMOS Signaling Interface Using Current Integrating Receivers," IEEE Journal of Solid-State Circuits, Vol. 32, No. 5, May 1997, pp. 681-690.
	J	

Examiner	<i>SJ</i>	Date Considered	<i>9/1/03</i>
----------	-----------	-----------------	---------------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.



PTO/SB/08A (08-03)

Approved for use through 07/31/2006. OMB 0651-0031  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE  
a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

**(Use as many sheets as necessary)**

Sheet

of 2

**Complete if Known**

Application Number	09/654,643
Filing Date	09/05/2000
First Named Inventor	Pak Shing Chau
Art Unit	2631
Examiner Name	Bayard, Emmanuel
Attorney Docket Number	RA-194 (RA194.P.US)

## **U. S. PATENT DOCUMENTS**

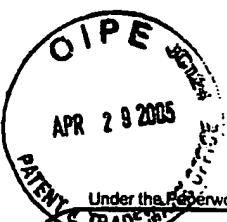
## **FOREIGN PATENT DOCUMENTS**

Examiner Signature		Date Considered	5/12/2015
--------------------	---	-----------------	-----------

**\*EXAMINER:** Initial if reference considered whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments or amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Approved for use through 07/31/2006. OMB 0651-0031  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PATENT & TRADEMARK OFFICE  
Substitute for Form 1449/PTO

*Complete if Known*

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>		Application Number	09/654,643
		Filing Date	09/05/2000
		First Named Inventor	Pak Shing Chau
		Art Unit	2631
		Examiner Name	Bayard, Emmanuel
Sheet	2	of	2
		Attorney Docket Number	RA-194 (RA194.P.US)

#### NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
<i>AS</i>	2	CHOI, JONG-SANG et al., "A CMOS 3.5Gbps Continuous-time Adaptive Cable Equalizer with Joint Adaptation Method of Low-Frequency Gain and High-Frequency Boosting." 2003 Symposium on VLSI Circuits Digest of Technical Papers. Pgs. 103-104.	
<i>AS</i>	3	SHAKIBA, MOHAMMAD HOSSEIN, "WP 23.3 A 2.5Gb/s Adaptive Cable Equalizer." 1999 IEEE International Solid-State Circuits Conference. Pages 396-397.	
	4	BAKER, ALAN J., "FA 10.7: An Adaptive Cable Equalizer for Serial Digital Video Rates to 400Mb/s." 1996 IEEE International Solid-State Circuits Conference. Pages 174-175.	
	5	KUDOH, YOSHIHARU et al., "A 0.13- $\mu$ m CMOS 5-Gb/s 10-m 28 AWG Cable Transceiver with No-Feedback-Loop Continuous-Time Post-Equalizer." IEEE Journal of Solid-State Circuits, Vol. 38, No. 5, May 2003. Pages 741-746.	
	6	GRANBERG, TOM, "Handbook of Digital Techniques for High-Speed Design." Cover and pub. pg., pgs. 211-226.	
	7	FARJAD-RAD, RAMIN et al., "0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization." 2003 Symposium on VLSI Circuits Digest of Technical Papers. 4 Pages.	
	8	STOJANOVIC, VLADIMIR et al., "Adaptive Equalization and Data Recovery in a Dual-Mode (PAM2/4) Serial Link Transceiver." June 2004. 4 pages. Rambus, Inc., Los Altos, CA 94022, USA and Department of Electrical Engineering, Stanford University, CA 94305, USA.	

Examiner Signature	<i>[Signature]</i>	Date Considered	<i>5/6/05</i>
--------------------	--------------------	-----------------	---------------

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.